

**REMARKS**

Claims 10-18 and 20 are pending in the present application. Claims 10 and 20 have been amended. Claim 19 has been canceled.

**Information Disclosure Statement**

The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement filed concurrently herewith, and to confirm that the documents listed therein have been considered and will be cited of record in the present application.

**Drawings**

Applicants note the Examiner's acceptance of the Replacement drawings submitted along with the Request for Reconsideration dated April 28, 2006.

**Claim Objections**

Claim 19 has been objected to under 37 C.F.R. 1.75(c), as allegedly being of improper dependent form for failing to further limit the subject matter of the previous claim. Although Applicants do not necessarily concede that this objection is proper, claim 19 has been canceled merely to advance prosecution of this application.

**Claim Rejections-35 U.S.C. 103**

Claims 10, 14-17 and 19 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of the Zenner et al. reference (U.S. Patent No. 6,246,010). This rejection is respectfully traversed for the following reasons.

The method of mounting a semiconductor device on a mounting substrate of claim 10 includes in combination among other features "providing the semiconductor device as including a semiconductor element, a sealing resin, and a plurality of terminals on the sealing resin, the semiconductor element having a thickness of 200 µm or less, a first surface wherein circuitry is formed, a second surface, and side surfaces positioned between the first and second surfaces, the sealing resin having a thickness equal to or greater than half a thickness of the semiconductor element so that the first surface is sealed by the sealing resin and the second and side surfaces are not sealed by the sealing resin, each of the plurality of terminals being electrically connected to the circuitry". Applicants respectfully submit that claim 10 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The Examiner has asserted that Applicants' admitted prior art Figs. 9-12 disclose all the features of claim 10, except for a semiconductor element having a thickness of 200 µm or less, and sealing resin having a thickness equal to or greater than half a thickness of the semiconductor element. In an effort to overcome this acknowledged deficiency, the Examiner has relied on Fig. 3A of the Zenner et al. reference as

disclosing a semiconductor element 12 and "a sealing resin" (adhesive film). The Examiner has further asserted that it would have been obvious to use semiconductor element thickness and adhesive film thickness as in the teaching of the Zenner et al. reference with the method of Applicants' admitted prior art, to create a high-density electronic package of improved mechanical and thermal properties. Applicants respectfully disagree for the following reasons.

As described in column 3, lines 46-52 of the Zenner et al. reference with respect to Fig. 1, circuit package 10 combines a thinned active semiconductor component 12 mounted on a flexible substrate 14 using an adhesive layer 16. Adhesive layer 16 is shown in Fig. 1 of the Zenner et al. reference as a layer separate from semiconductor component 12 and substrate 14. As described further in column 3, lines 60-66 of the Zenner et al. reference, adhesive layer 16 may be applied on the underside of the electronic component 12, and bonding pads such as gold bumps on the underside of the semiconductor component may push through the adhesive layer 16 to make contact with conductive circuit traces 18 on the circuit substrate 14. This may be understood in Fig. 3A of the Zenner et al. reference, wherein interconnect pads 15 of semiconductor component 12 are shown as pushing through adhesive layer 16.

In contrast, the method of mounting a semiconductor device of claim 10 includes in combination providing a semiconductor device as including a semiconductor element, a sealing resin, and a plurality of terminals that are on the sealing resin. This semiconductor device is then fixed to the mounting substrate by a heat treatment. The

Zenner et al. reference clearly fails to disclose these features, because adhesive layer 16 is merely a layer applied between semiconductor component 12 (which previously has bonding pads thereon) and circuit substrate 14, to affix semiconductor component 12 to circuit substrate 14 . Adhesive layer 16 of the Zenner et al. reference is not a sealing resin, and does not have a plurality of terminals thereon. Since adhesive layer 16 of the Zenner et al. reference cannot be interpreted as the sealing resin of claim 10, the prior art as relied upon by the Examiner does not disclose or suggest a relationship between semiconductor element thickness and sealing resin thickness, and more particularly does not disclose such a relationship that would reduce the occurrence of cracks at a junction between a semiconductor element and a mounting substrate. Applicants therefore respectfully submit that the method of mounting a semiconductor device on a mounting substrate of claim 10 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 10 and 14-17 is improper for at least these reasons.

With further regard to this rejection, on page 4 of the current Office Action dated July 10, 2006, the Examiner has asserted that the Capote et al. reference (U.S. Patent No. 6,297,560) discloses a plurality of terminals that are solder balls 14, and has asserted that the heat treatment comprises reflow of solder balls. The Examiner has consequently rejected claims 14-17. However, the Capote et al. reference has not been cited as a basis for this rejection. Moreover, even assuming for the sake of argument that the Capote et al. reference was properly cited (which Applicants do not

concede), the particularly relied upon teaching would not overcome the above noted deficiencies of the Zenner et al. reference as combined with Applicants admitted prior art. Applicants therefore respectfully submit that this rejection of claims 14-17 is improper for at least these additional reasons.

Claim 11 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art and the Zenner et al. reference, in further view of the Takahashi et al. reference (U.S. Patent No. 6,153,448). Applicants respectfully submit that the Takahashi et al. reference as relied upon does not disclose a semiconductor device having a semiconductor element which has a thickness of 200  $\mu\text{m}$  or less, and a sealing resin which has a thickness equal to or greater than half the thickness of the semiconductor element. The Takahashi et al. reference does not disclose or suggest a relationship between semiconductor element thickness and sealing resin thickness, and more particularly does not disclose such a relationship that would reduce the occurrence of cracks at a junction between a semiconductor element and a mounting substrate. Applicants therefore respectfully submit that claim 11 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 11 is improper for at least these reasons.

Claims 12, 13, 18 and 20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art and the Zenner et al. reference, in further view of the Capote et al. reference (U.S. Patent No. 6,297,560). Applicants respectfully submit that the Capote et al. reference does not disclose thickness of chip

10, and does not disclose thickness of an encapsulant material 22 or 37 in relation to thickness of chip 10. The Capote et al. reference does not disclose or suggest a relationship between semiconductor element thickness and sealing resin thickness, and more particularly does not disclose such a relationship that would reduce the occurrence of cracks at a junction between a semiconductor element and a mounting substrate. Applicants therefore respectfully submit that claims 12, 13, 18 and 20 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection is improper for at least these reasons.

**Conclusion**

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

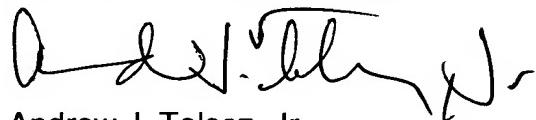
Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicants hereby petition for an extension of two (2) months to December 10, 2006, for the period in which to file a response to the outstanding Office Action. The required fee of \$450.00 should be charged to Deposit Account No. 50-0238.

Serial No. 10/718,549  
OKI.136D3  
Amendment dated November 29, 2006

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



Andrew J. Telesz, Jr.  
Registration No. 33,581

One Freedom Square  
11951 Freedom Drive, Suite 1260  
Reston, Virginia 20190  
Telephone No.: (571) 283-0720  
Facsimile No.: (571) 283-0740